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09/516,162	02/29/2000	Koji Hirayama	572.38256X00	1546

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EXAMINER
PHAN, TRI H

ART UNIT	PAPER NUMBER
2661	6

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/516,162	HIRAYAMA ET AL.	
	Examiner	Art Unit	
	Tri H. Phan	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- Regarding Claim 3, the recitation "*plural kinds of processors*" in Line 2 and 4, "*other processors*" in Lines 5-6, 9 and 11, "*processor*" in Line 8, are vague and indefinite because it is unclear whether the limitations refer to "*signal processors*" of the control processor or "*the control processor*" as defined in the parent claims (claims 1 and 2). Similar problem exists in Claim 12, Lines 5-7 and 9.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ueda et al.** (U.S.5,359,600) in view of **Kato** (U.S.6,529,523).

- Claims 3 and 12 are rejected under 35 U.S.C. 112, second paragraph, set forth in this Office action, as in Part 3 above, but in the interest of expediting the examination process, the examiner will interpret the claimed inventions as 'plural kinds of signal processors' in place of "*plural kinds of processors*" in Line 2 and 4, 'other signal processors' in place of "*other processors*" in Lines 5-6, 9 and 11, 'signal processor' in place of "*processor*" in Line 8. Similar replacing is for claim 12.

- In regard to claims 1 and 9, **Ueda** discloses in Figs. 1-4 and in the respective portions of the specification that the method and system for the ATM switching network ("*switching system*") includes a plurality of incoming trunk circuits with STM-ATM receive interface unit ("*plural kinds of interfaces*") which convert the STM-N and ATM incoming signals ("*plural kinds of networks*") into ATM cells ("*ATM cells*") inputted at the inlets ("*input lines*") of the ATM self-routing switch and outputted at the outlets ("*output lines*") of the ATM self-routing switch to the one of the outgoing trunk circuits(For example see Col. 2, Lines 11-61) specified by the VPI ("*based on the header information of the ATM cell*") as disclosed in Col. 3, Lines 33-36. **Ueda** does discloses about the maintenance and management system provided to determine

and control the routing plan of the traffic in the system, but fails to specially disclose about "*plural kinds of signal processors*". However, such implementation is known in the art.

For example, **Kato** discloses in Figs. 1-8, 13 and in the respective portions of the specification about the converting circuits and bandwidth management apparatus in the mixing STM and ATM networks, wherein the processor CPU at each line interfaces ("*plural kind of signal processors*") controls the process at each unit such as the converting circuit and timing circuit for the STM signals based on the information of the header (For example see Col. 5, Lines 17-51; Col. 6, Lines 48-57; Col. 8, Lines 19-52; Col. 9, Line 15 through Col. 10, Line 16.

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to implement the invention as taught by **Kato** by using each processor for each switch unit, e.g. 'incoming trunks', in the **Ueda**'s system, with the motivation being to improve the ability to convert and manage the bandwidth and timing for each unit in the mixing network, e.g. STM and ATM networks.

- Regarding claims 2, 8, 11 and 17, **Ueda** does discloses about the maintenance and management system provided to determine and control the routing plan of the traffic in the system, but fails to specially disclose about "*control processor*" . However, such implementation is known in the art.

For example, **Kato** discloses each system management processor ("*control processor*") at each sending/receiving switch, i.e. controller 15 in Fig. 1, control the overall system by communicating with CPUs of the ATM and STM switches as specified in Col. 5, Lines 24-26; or with the write controller 39, read controller 40 and read/write controller ("*plural kinds of*

processors") as disclosed in Fig. 3; Col. 7, Line 29 through Col. 8, Line 18; each provides different control for reading and writing of address data to and from the control memory at period of the time slots ("*executing different processing*"); the routing unit 56 ("*second ATM switch*") as disclosed in Fig. 8, Col. 9, Line 15 through Col. 10, Line 16; adds the destination information into the header for performing switching cells to destination.

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to implement the invention as taught by **Kato** by using the system management processor in the maintenance and management system **Ueda**'s system, with the motivation being to improve the ability to centralize the control of the overall system such as the bandwidth and timing in the mixing networks, e.g. STM and ATM networks.

- In regard to claims 3 and 12, **Ueda** further fails to disclose about the plural kinds of processors for executing different processing and the second ATM switch for transferring information to other processor based on the header information of the ATM cell. However, such implementation is known in the art.

For example, **Kato** discloses about the write controller 39, read controller 40 and read/write controller ("*plural kinds of processors*") as disclosed in Fig. 3; Col. 7, Line 29 through Col. 8, Line 18; each provides different control for reading and writing of address data to and from the control memory at period of the time slots ("*executing different processing*"); the routing unit 56 ("*second ATM switch*") as disclosed in Fig. 8, Col. 9, Line 15 through Col. 10, Line 16; adds the destination information into the header for performing switching cells to destination.

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to implement the invention as taught by **Kato** by using different controllers for different processing and routing unit for each switch unit, e.g. 'incoming trunks', in the **Ueda**'s system, with the motivation being to improve the ability to perform different processing, such as read and writing destination data into the cell header in order to perform the routing cells for each unit in the mixing network, e.g. STM and ATM networks.

- Regarding claims 4, 6-7, 13 and 15-16, **Ueda** further fails to disclose about the signal processors form and output the ATM cells having header destined to other processors. However, such implementation is known in the art.

For example, **Kato** discloses each processor CPU ("*signal processors*") at each sending/receiving switch as disclosed in Figs. 1, 3, 8 and 9; Col. 7, Line 29 through Col. 8, Line 18; forms the ATM cells by using the converting circuit and the routing unit 56 as disclosed in Fig. 8, Col. 9, Line 15 through Col. 10, Line 16; using the destination add-on unit for adding the destination information into the cell header for performing switching cells to destination.

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to implement the invention as taught by **Kato** by using the processor CPU and routing unit for each switch unit, e.g. 'incoming trunks', in the **Ueda**'s system, with the motivation being to improve the ability to convert STM data to ATM cells and perform the routing cells for each unit in the mixing network, e.g. STM and ATM networks.

- In regard to claims 5 and 14, the combination of the **Ueda** and **Kato**'s system does disclose about the mixing networks, e.g. STM and ATM networks, but fails to disclose about the IP network. However, Internet Protocol network is well known in the art for transporting the IP packets. Therefore, it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to use an IP interface for converting the IP packets into ATM cells in the incoming trunk circuit of the **Ueda** and **Kato**'s system.

- Regarding claim 10, **Ueda** further discloses the incoming trunk circuit ("*first interface*") receives STM-N signal, converts to ATM cell, switches through the ATM self-routing switch ("*ATM switch*"), and transmits through the outgoing trunk circuit to other communication network as disclosed in Fig. 1; Col. 1, Lines 31-63; Col. 2, Lines 11-61.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Van Grinsven et al. (U.S.6,414,967), **Watanabe** (U.S.5,771,231) and **Mano** (U.S.6,012,151) are all cited to show devices and methods for improving switching architectures with ATM network, which are considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tri H. Phan, whose telephone number is (703) 305-7444. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W. Olms can be reached on (703) 305-4703.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 305-3900.

Tri H. Phan
July 27, 2003